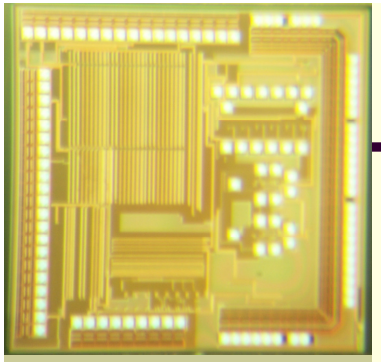
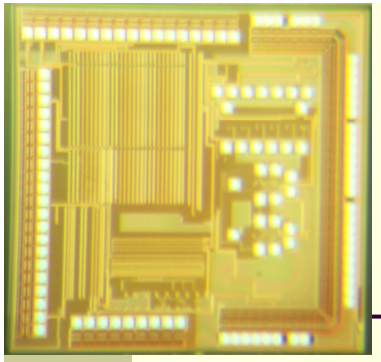


# HIVAC
## (High Voltage chip Analysis Circuit)

Aaron Koga

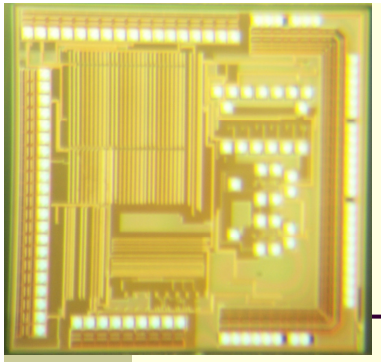
May 8, 2007

Physics 476



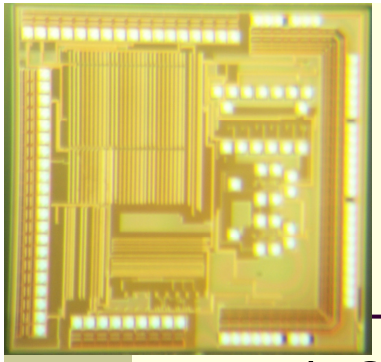
# OUTLINE

- Introduction
  - PanSTARRS
  - High Voltage Chip
- HIVAC design, layout
- Current status
- Future plans



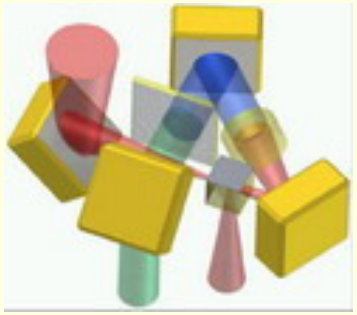
# INTRODUCTION (PanSTARRS)

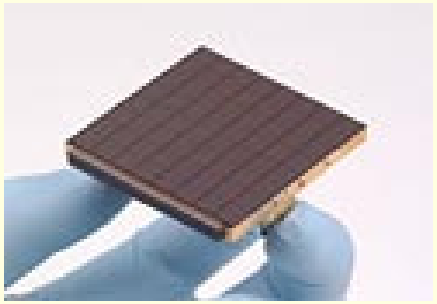
- University of Hawaii Institute for Astronomy
- Panoramic Survey Telescope And Rapid Resonse System
  - *"…discover and characterize Earth-approaching objects, both asteroids & comets, that might pose a danger to our planet."*
- 4 optical systems
- Observe entire sky few times/month

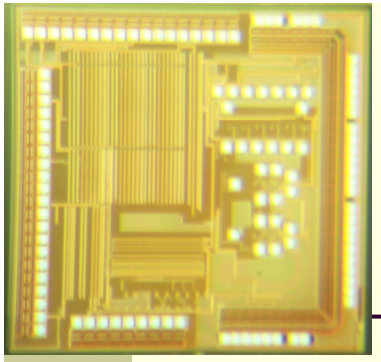


# INTRODUCTION (PanSTARRS Optical System)

- 1.8 m mirror
- OTA (Orthogonal Transfer Array)
  - 8x8 array of CCD's (Charge Coupled Devices)
  - 1.4 gigapixels
  - Compensate for atmospheric distortion (tip-tilt corrections)
- MOTA (Mini-OTA)
  - 2x2, some testing of advanced features
  - Keep cool to make measurements

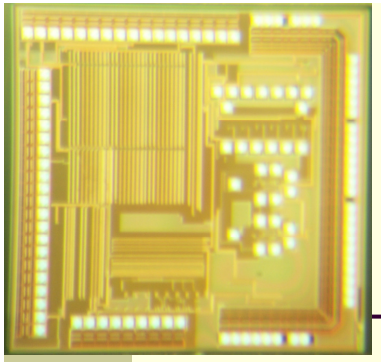






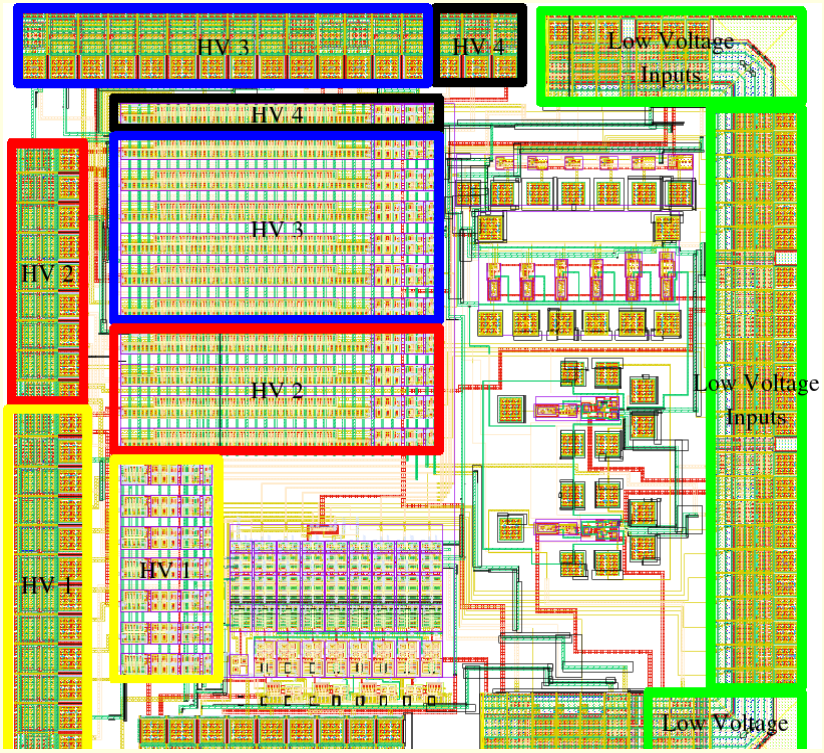
# INTRODUCTION (PanSTARRS & HV Chip)

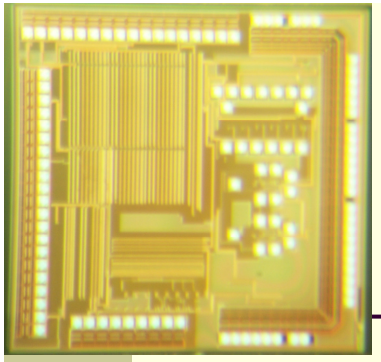
- Want to make OTA controls automated
- STARGRASP
  - Controller to read OTA
- Problem: OTA uses higher voltage logic levels
- Solution: CID HV Chip designed (CMOS Interface Device for High Voltage)
  - High drive strength
  - Integration with CCD



# INTRODUCTION (HV Chip)

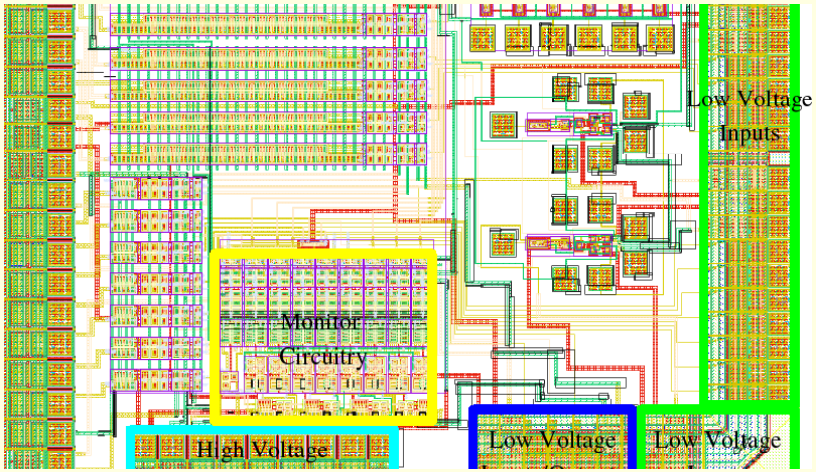
- 0 to 3.3V input, -3.3 to 16.7V output
- Expect to drive 50pF & 1000pF loads
- 4 different high voltage levels

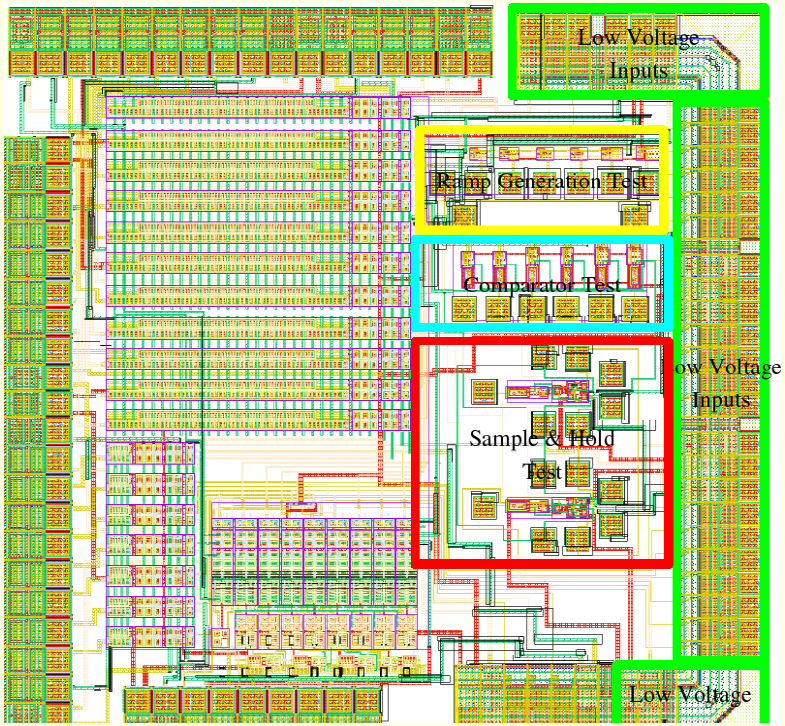


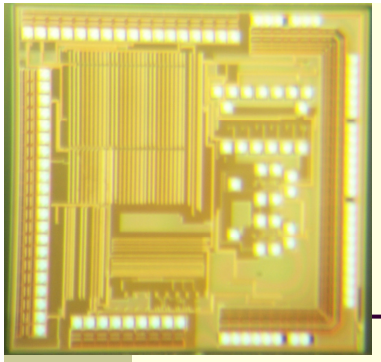


# INTRODUCTION (HV Chip)

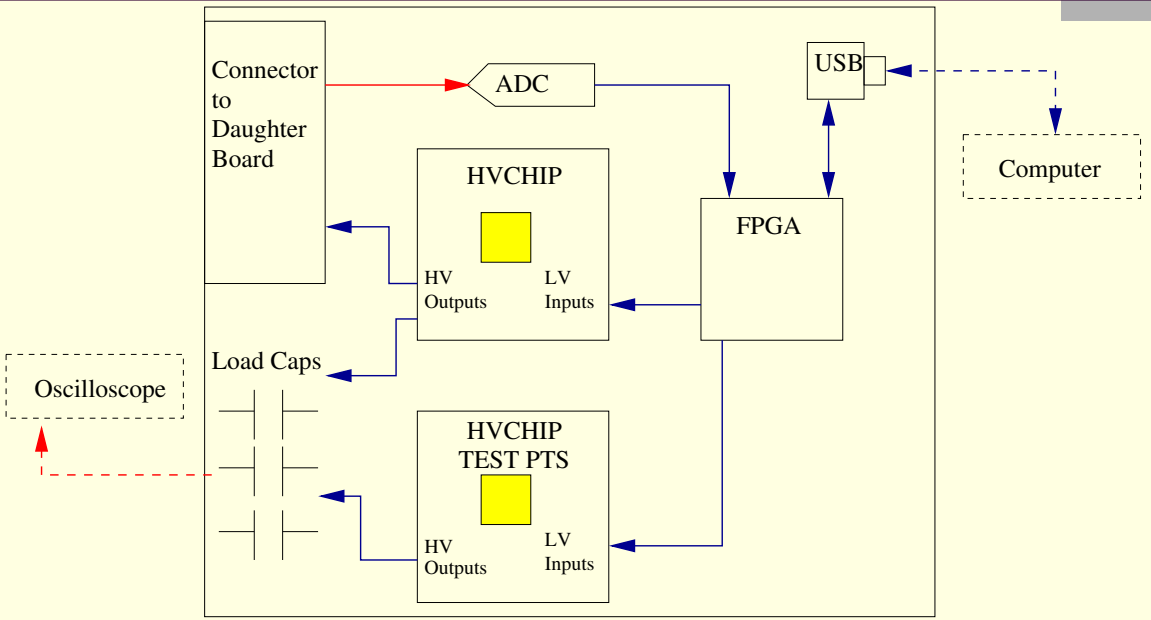
- Monitor outputs for logic to MOTA
- Test structures for future ADC



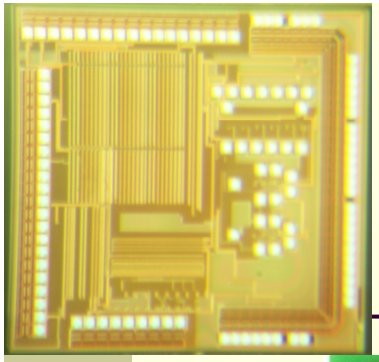





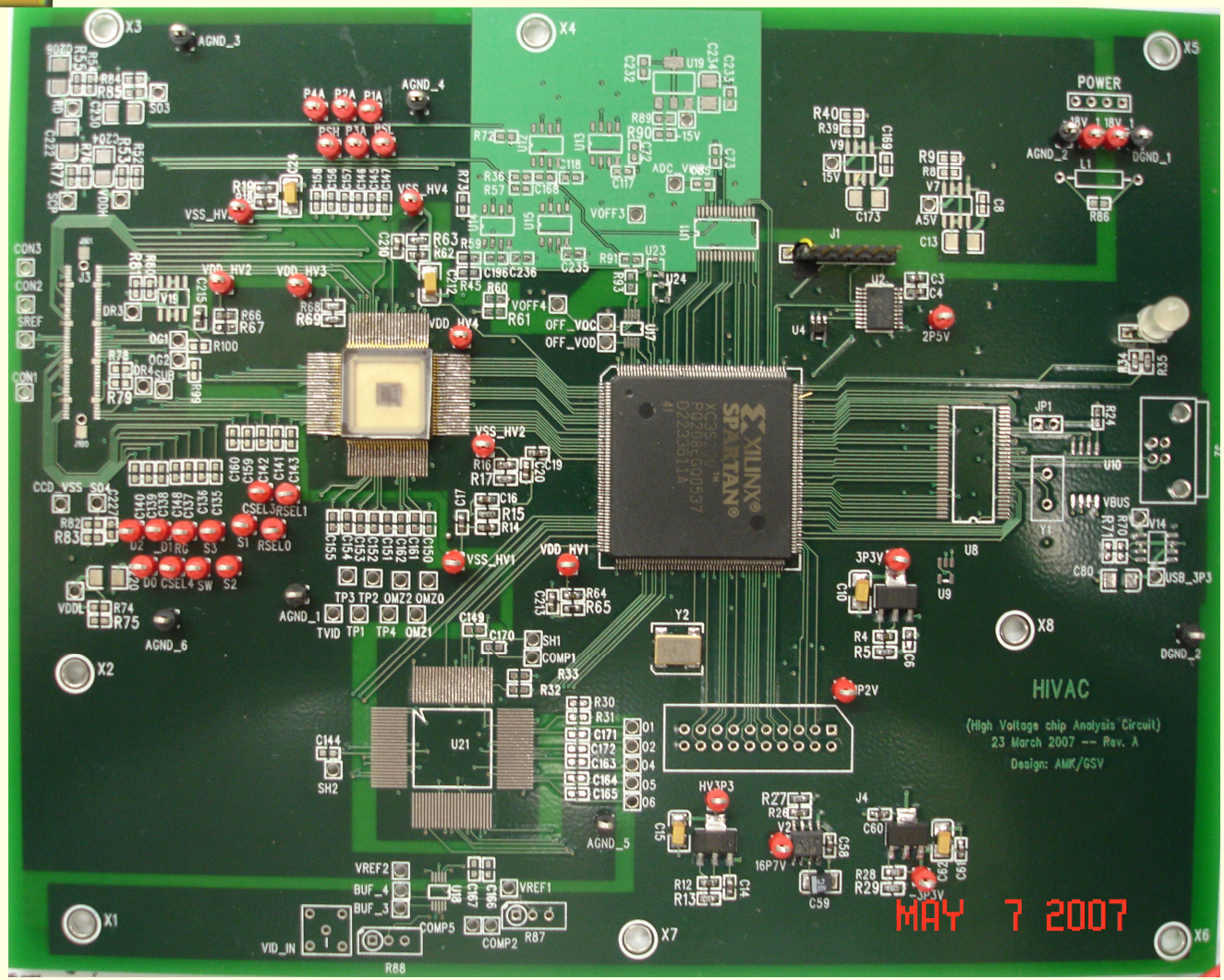
# HIVAC (Overview)

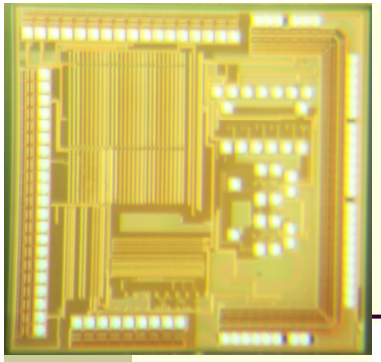



- Test HV Chip into capacitive load
  - rise time, operating range, etc
  - Measure with oscilloscope
- Connection to daughter board with MOTA
- USB communication



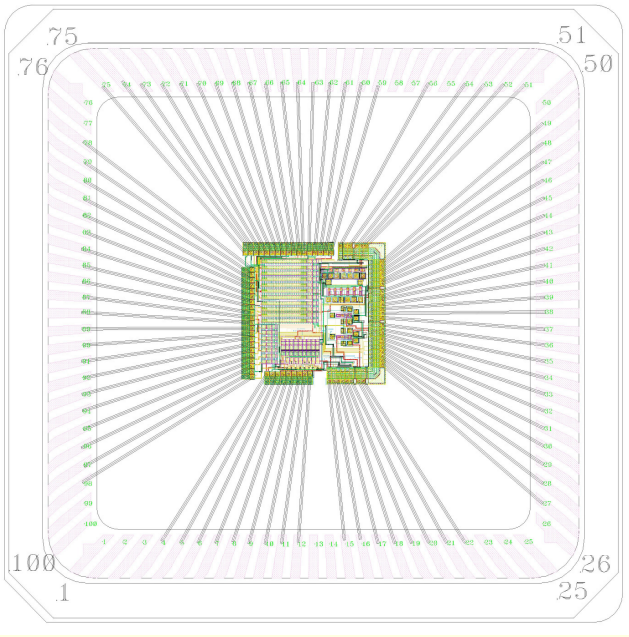
# HIVAC (Overview)

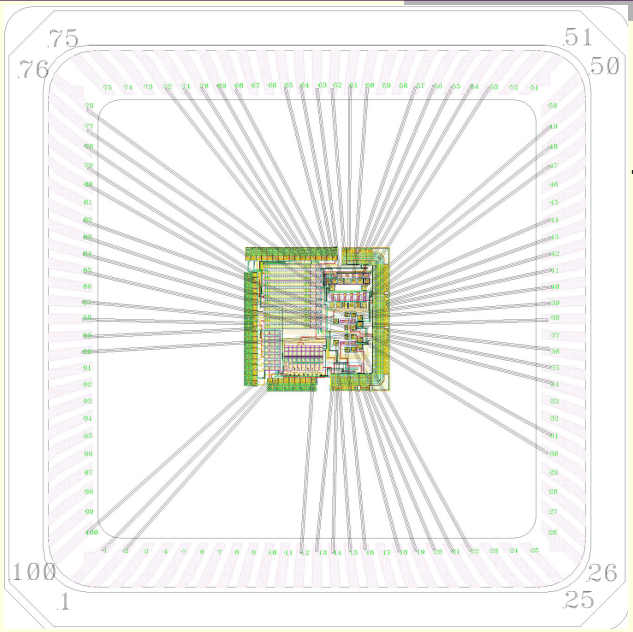




# HIVAC
# (HV Chip Bonding)

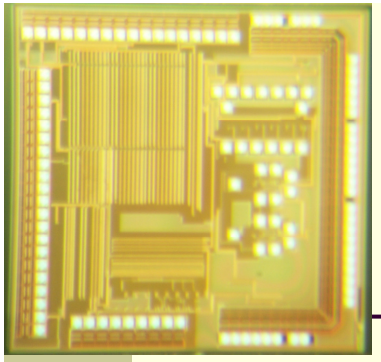
Functional



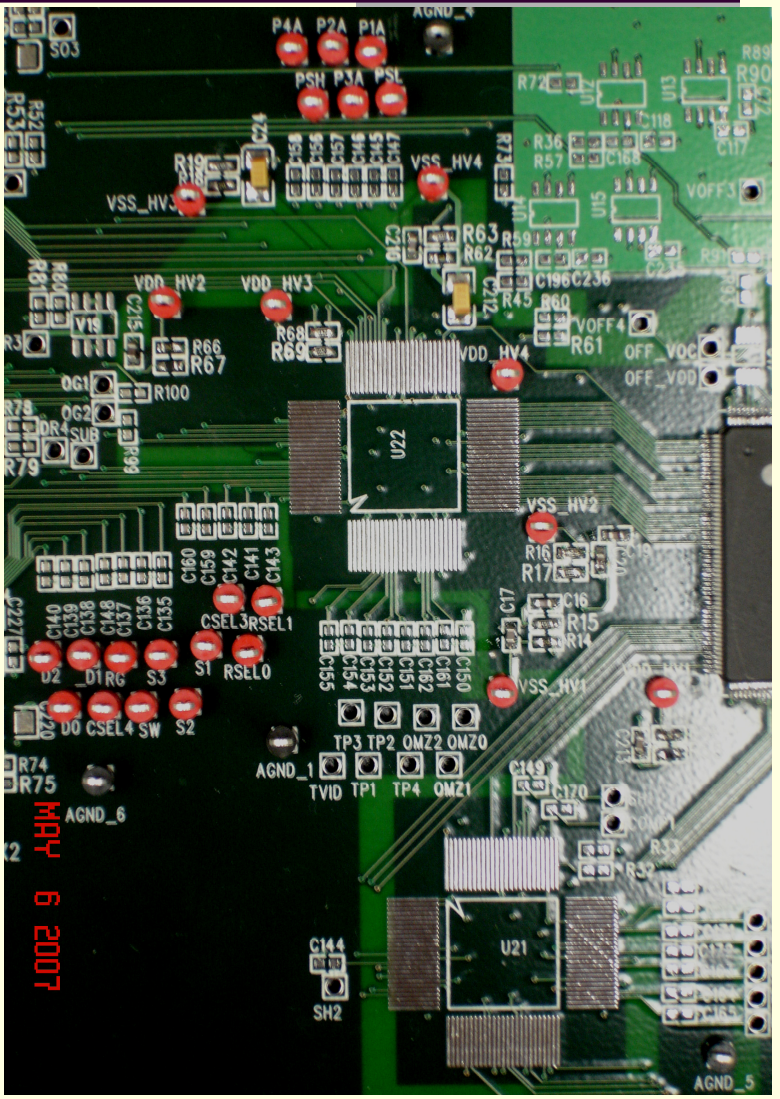

Test

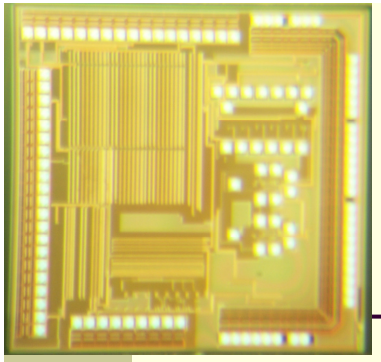
- 113 pads on chip, 100 pin package → 2 bonding layouts
- Functional: control of MOTA & monitor outputs
- Test: test structures



# HIVAC
# (HV Chip Bonding)

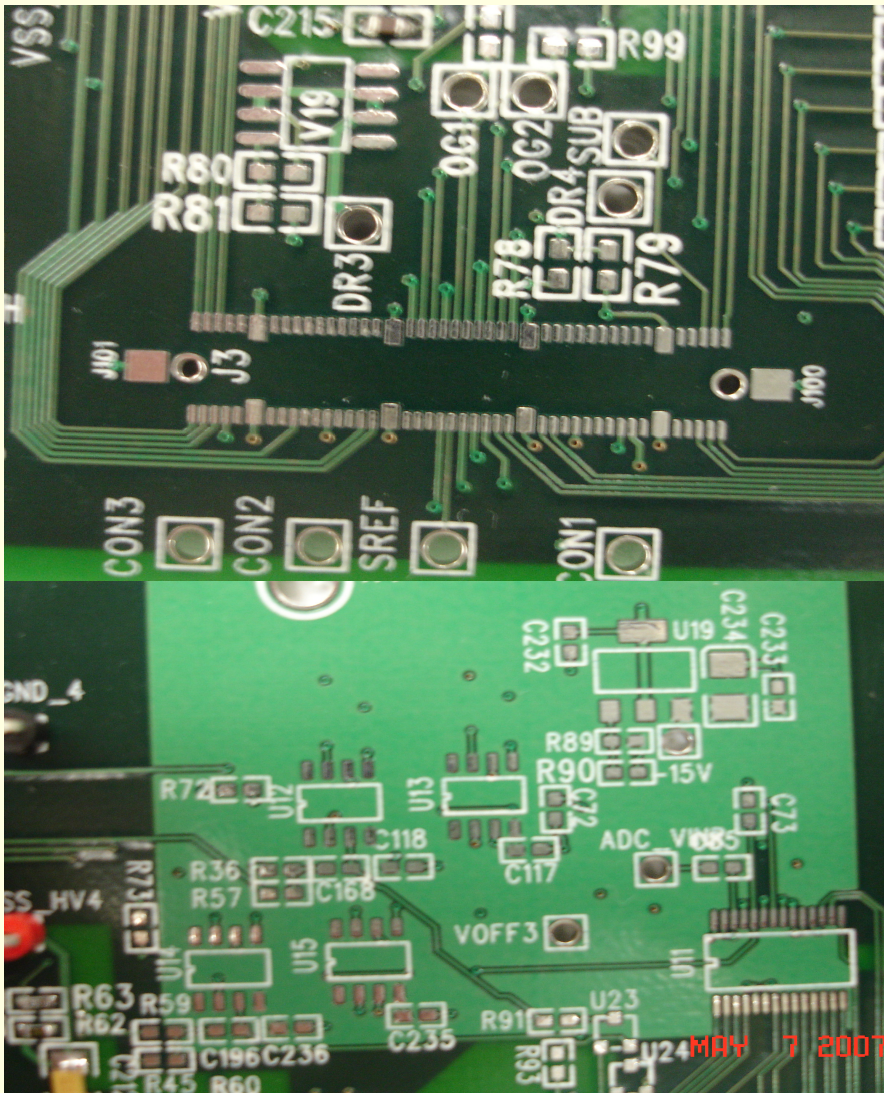
- 36 load caps

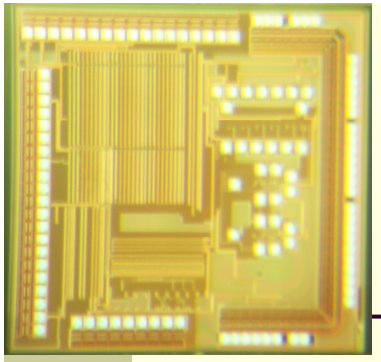




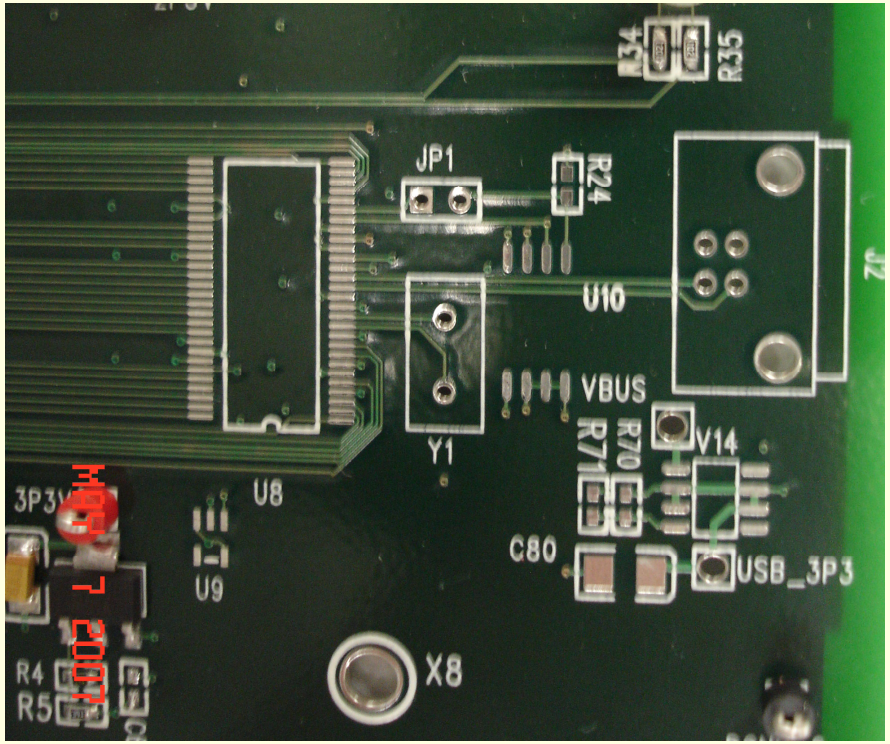
# HIVAC (Connector/ADC)

- 18 signals output to daughter
- 4 signals in from daughter
- ADC / level shifting
  - IFA design
  - 16 bit ADC



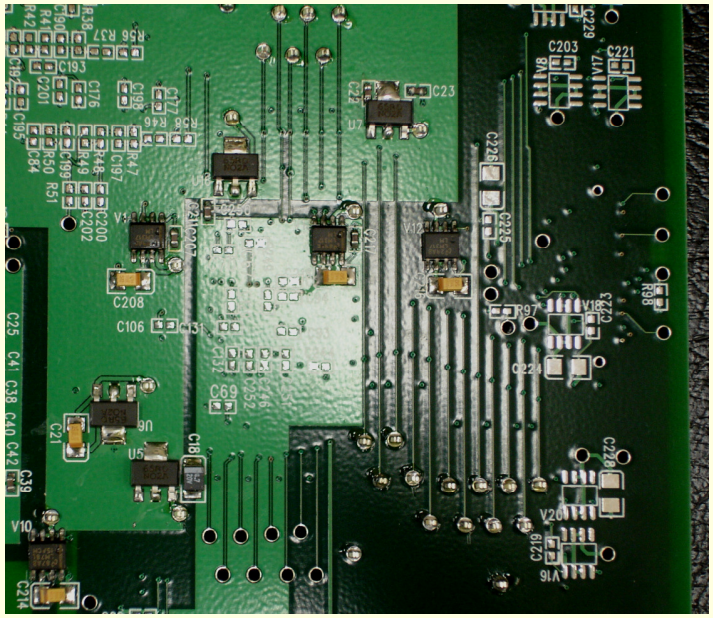


# HIVAC (USB)

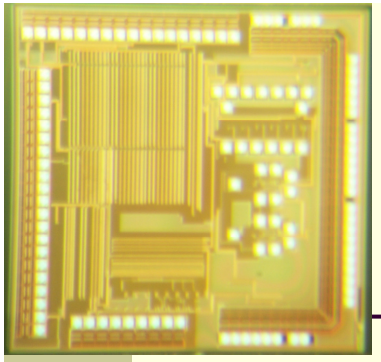



- Cypress USB

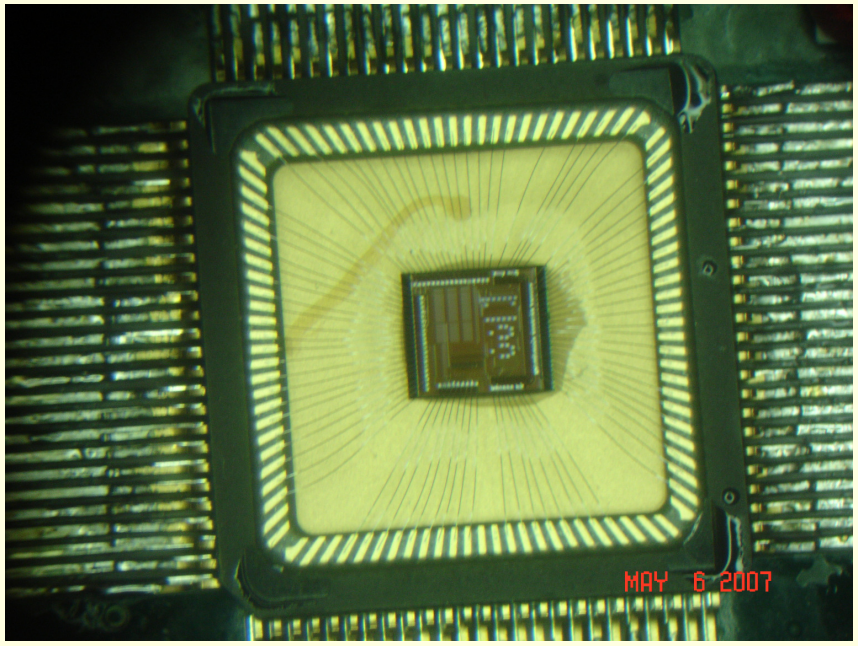
# HIVAC
# (Power Supplies)



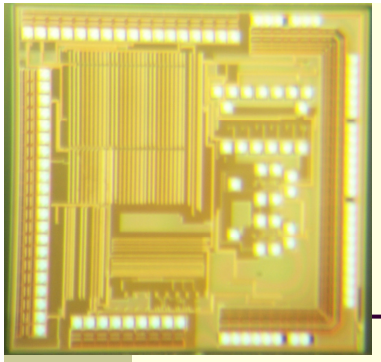
- 26 total
  - 8 for general use
  - 10 for HV Chips
  - 8 for daughter board
  - +20V, -20V to from supply



# CURRENT STATUS

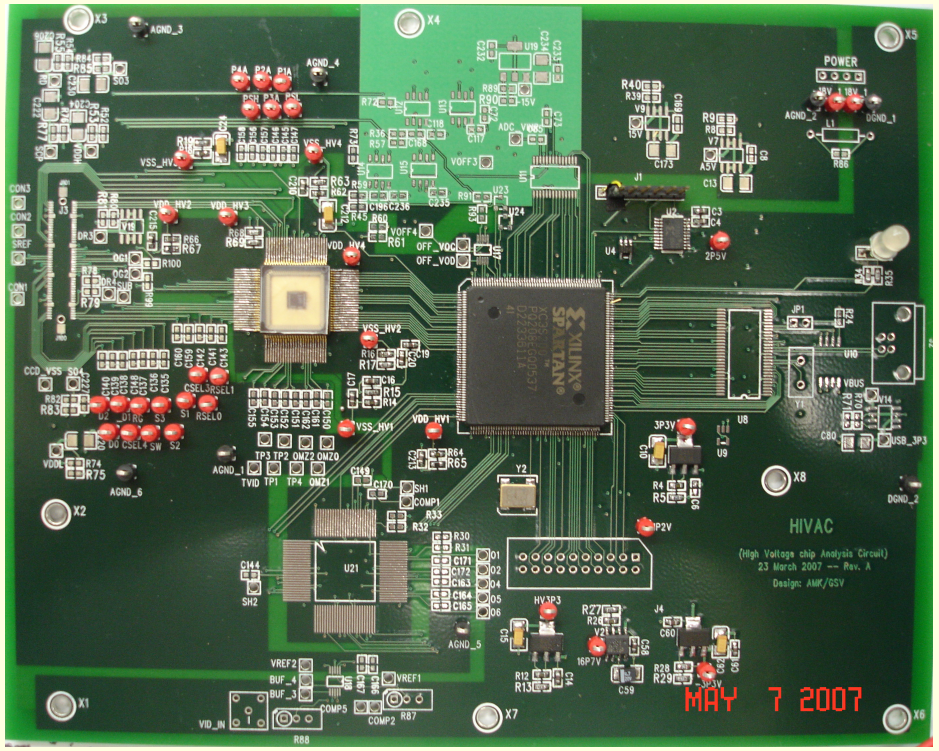


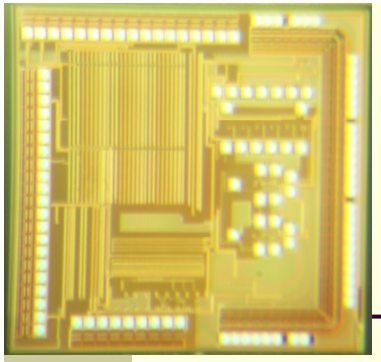

- One HV Chip bonded
- Functional: daughter board outputs



# CURRENT STATUS

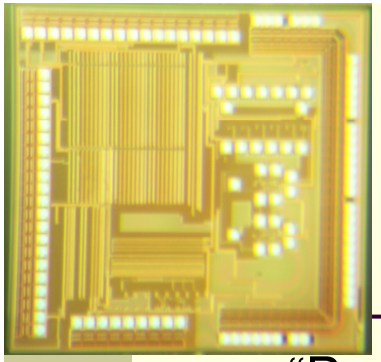
- Board partially assembled
- No connector & ADC circuit
- No USB
- Attempting to get HV Chip to work





# FUTURE PLANS

- Board assembly as needed
- Testing of all 36 outputs into capacitive loads
- Firmware/Software
  - ADC readout
  - USB control
- Testing with MOTA



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